Meeting the Challenges of the New Millennium: The Universal Relay

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Challenges Facing the Power Industry...

- Increased competition due to de-regulation
  - *Find new competitive advantages.*
- Industry segmentation into generation, transmission, distribution & services
  - *Power quality and reliability responsibility at the segment interfaces - who pays?*
- Cost effectiveness and efficiency
  - “*Do more with less*” in all areas.
Challenges Facing Relay Designers...

• Leverage technology to provide new competitive advantages (e.g. information technology)
  – *From ‘Silent Sentinels’ to ‘Gregarious Guardians’*

• Provide a ‘universal relay’ solution
  – *A common tool for protection, metering, monitoring and control across the entire power system.*

• Cost effectiveness and efficiency
  – “*One solution that does it all - cost effectively*”
Performance driven by competitive PC market.

Benefits:
- Industrial spin-offs of mature PC technology.
- Emergence of one dominant communications technology.
Cost effective processing power available: < $1/MIP.
Technology Delivers...

• **Cost-effective processing capabilities**
  – Handles high-end performance requirements and low-end cost effectiveness requirements

• **Cost-effective high-speed communications**
  – 1Mbps serial port (< $50)
  – 10Mbps Ethernet via fiber (< $100)
  – 100Mbps Ethernet via fiber (< $200)

• The above two factors allow for a ‘universal relay’ which can:
  • Provide both low-end and high-end applications cost effectively.
  • Provide high-speed network communications cost effectively.
An architecture which can accommodate both cost and performance requirements.
Universal Relay Architecture - ‘Modularity’

High-Speed Data Bus

- Power Supply
- CPU
- DSP & Magnetics
  - DSP processor + CT/VTs
- DIGITAL I/O
  - Status Inputs / Control Outputs
- ANALOG I/O
  - Analog Transducer I/O
- COMMUNICATIONS
  - Ethernet, HDLC, UART

LED Modules
LED Modules
LED Modules
Display
Keypad

Modular HMI Panel
Module Functionality/Requirements

**Power Supply Module**
- Wide input range
  - 24 - 300 VDC
  - 20 - 265 VAC
- High Efficiency SMPS
  - > 80%
- High Reliability
  - > 50yrs MTBF

**CPU Module**
- High-speed 32-Bit RISC Processor
  - > 50 MIPS
  - Instruction & Data Caches
- Support for high-speed memory: SDRAM
  - > 33 MHz
- Large memory capacity and expansion
  - > 8 MB

**DSP + Magnetics Module**
- Modular CT/VT configurations
  - up to 8 CT/VTs
- High-speed digital sampling
  - > 64 samples / power cycle
- High-speed Digital Signal Processor
  - > 32 MIPS

**Digital I/O Module**
- Control outputs
  - Solid State
  - Electromechanical - multiple types
  - Fast activation speeds (< 4ms)
- Status inputs
  - Dry and Wet contacts
  - 18 - 300 VDC
  - Fast detection speeds (< 4ms)
Module Functionality/Requirements

**Analog I/O Module**
- Transducer type inputs
  - ± dcmA
  - ± Voltage
  - Resistive
- Outputs for Legacy SCADA
  - ± dcmA
- Support multiple I/O configurations

**Communications Module**
- High-speed Serial
  - Asynchronous (9600 - 115K Baud)
  - Synchronous (56K - 256K Bps)
  - Fiber Optical (Single/Multi mode)
  - Channel Redundancy
- High-speed Network (LAN)
  - Ethernet/Fiber Optical
  - Channel Redundancy
  - Wireless

**High-Speed Data Bus**
- High-Speed Parallel Data Bus: 80 - 100 Mbytes/sec
- High-Speed Serial Communications Bus: 10Mbps
- High-Speed Inter-Processor Serial Data Bus: 16Mbps

Multiple buses prevent bottlenecks
Architecture - Physical Realization

Prototype

19” Chassis (Enclosure)

19” Chassis (Rear View)

Universal power supply
Central processing unit
Analog signal processor
Digital I/O unit
Analog unit
Communication module

Power Supply
CPU
Main Processor
DSP & Magnetics
Digital I/O
Analog Transducer I/O
Status Inputs / Control Outputs
Communications (Ethernet, HDLC, UART)
High-Speed Data Bus
19'' Chassis (Enclosure)
19'' Chassis (Rear View)
Architecture - Modular ‘Plug n Play’

- Module draw-out method

- Field wiring is left undisturbed

CT Shorting ‘Clips’

High-Speed Data Bus
Architecture - ‘Configurability’

Configurable I/O via sub-modules

Sub-Modules
Architecture - ‘Scalability’

Scalability and Flexibility

Prototype

Minimum Configuration

Maximum Configuration

Prototype
Major functional elements required:

• Protection Elements
• Metering Elements
• Monitoring Elements
• Programmable Logic and I/O control
• Data and Event capture/storage
• HMI programmability
• Communications

Modular, flexible hardware architecture requires software to support it.
Modular Software: ‘Object Oriented’ Design

**Protection**

- TOC
- IOC
- Distance - Mho
- Distance - Quad
- Distance - Lens
- Differential - Xfrmr
- Differential - Bus
- Differential - Line
- Frequency - df/dt
- Frequency - Under
- Volts/Hz

**Class**

**Objects of the Class**
Building Applications: ‘Object Oriented’ Design

Classes

Protection  Metering  Control  Monitoring  HMI  Comms

Common Core Software

Application Software
A Common Platform: Modular H/W and S/W

Feeder
Line
Transformer
Generator
Busbar
Control
Power Quality
Application Software
Breaker-and-a-Half Scheme
Traditional Relay Application

Transformer Differential Relay

VT1, CT1, CT2, CT3, 50BF RELAY, Transformer, 50P, W, 87T

External Summation

VOLT, AMPS, 50P, W, 87T
Modular Architecture Solution

Power Supply

CPU

Main Processor

DSP & Magnetics
DSP processor + CT/VTs

DSP & Magnetics
DSP processor + CT/VTs

DIGITAL I/O
Status Inputs / Control Outputs

DIGITAL I/O
Status Inputs / Control Outputs

DIGITAL I/O
Status Inputs / Control Outputs

COMUNICATIONS
(Ethernet, HDLC, UART)

High-Speed Data Bus

AMPS CT1
AMPS CT2
AMPS CT3

50BF
50BF

50P
87T

VT1
CT1
CT2
CT3

VOLTS

WATT
Breaker-and-a-Half Scheme with Three-Winding Transformer
Modular Architecture Solution

Power Supply
CPU
DSP & Magnetics
DSP processor + CT/VTs
Main Processor
DSP & Magnetics
DSP processor + CT/VTs
DIGITAL I/O
Status Inputs / Control Outputs
DIGITAL I/O
Status Inputs / Control Outputs
 brackets)
DIGITAL I/O
Status Inputs / Control Outputs
COMMUNICATIONS
(Ethernet, HDLC, UART)

VT1
CT1
CT2
CT3
CT4

High-Speed Data Bus

VT1
CT1
CT2
CT3
CT4

VOLTS
CT1
AMPS
CT2
AMPS
CT3
AMPS
CT4

WATT
50BF
50BF
50BF
87T
50P
Busbar: 6 Feeder Section
Modular Architecture Solution: Busbar - 6 Feeders

Power Supply

CPU

Main Processor

DSP & Magnetics

DSP processor + CT/VTs

DSP & Magnetics

DSP processor + CT/VTs

DSP & Magnetics

DSP processor + CT/VTs

Digital I/O

Status Inputs / Control Outputs

Communications

Ethernet, HDLC, UART

VT1

CT1

CT2

CT3

CT4

CT5

CT6

High-Speed Data Bus

VOLTS

50BF

50BF

50BF

50BF

50BF

87B

27G

AMPS CT1

AMPS CT2

AMPS CT2

AMPS CT2

AMPS CT2

AMPS CT2

Digital I/O

Status Inputs / Control Outputs

Ethernet, HDLC, UART
High-Speed Communications allows for ‘private’ Remote I/O

Remote I/O
Busbar - 12 Feeders: Distributed Architecture

10Mbps Ethernet - Redundant Fiber

115 Kbps RS485

Remote I/O

Remote I/O
The two major goals of UCA 2.0:
• Device interoperability
• High-speed peer-to-peer communications
UCA 2.0: Performance Overview

- **RELAY “X”**
  - Event Detection Time (??)

- **LAN Response Time**
  - (< 4ms)

- **RELAY “Y”**
  - Response Time (??)

Event detection time and message processing time required by sending relay.

Worst case response time of LAN under ‘worst case’ conditions.

Message processing time and action response time required by receiving relay.
UCA 2.0: The Role of the ‘Universal Relay’

Ethernet
10/100Mbps

High-Speed Data Bus

Power Supply
CPU
Main Processor
DSP & Magnetics
DSP processor + CT/VTs
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COMMUNICATIONS
Ethernet, HDLC, UART
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Legacy Network
(Modbus - 9600 Bps)

Master
Slave 1
Slave n
Conclusions

• A modular architecture (both hardware and software) provides a ‘Universal Relay’ solution which can accommodate all applications in a flexible, scalable and cost effective manner.

• The ‘Universal Relay’ architecture allows for easy ‘upgradeability’ and future technological enhancements.